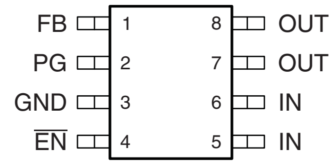
FEATURES

- **Qualified for Automotive Applications**
- **150-mA Low-Dropout (LDO) Voltage Regulator**
- **Dropout Voltage to 85 mV (Typ) at 150 mA (TPS76550)**
- **Ultra-Low 35-µA (Typ) Quiescent Current**
- **3% Tolerance Over Specified Conditions for Fixed-Output Versions**
- **Open-Drain Power Good Output**
- **Thermal Shutdown Protection**

D PACKAGE
(TOP VIEW)



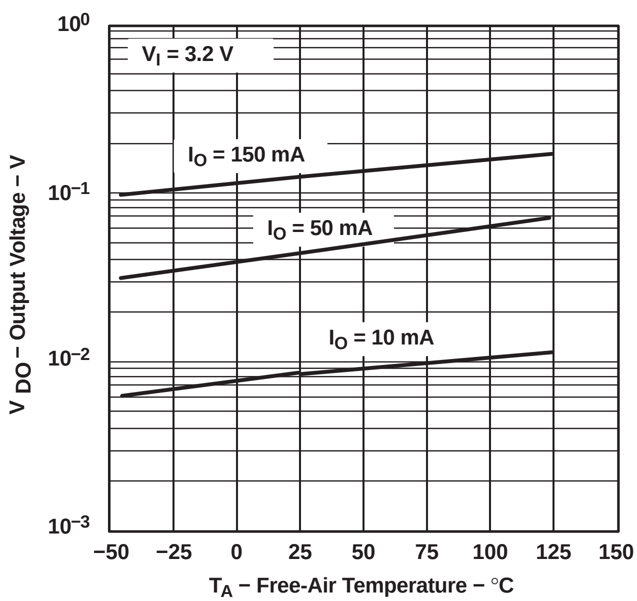
DESCRIPTION/ORDERING INFORMATION

This device is designed to have an ultra-low quiescent current and be stable with a 4.7-µF capacitor. This combination provides high performance at a reasonable cost.

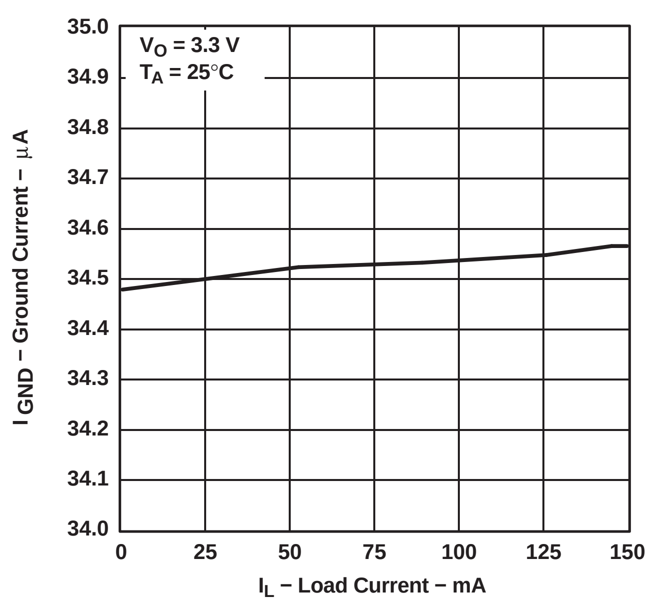
Because the PMOS device behaves as a low-value resistor, the dropout voltage is very low (typically 85 mV at an output current of 150 mA for the TPS76550) and is directly proportional to the output current. Additionally, since the PMOS pass element is a voltage-driven device, the quiescent current is very low and independent of output loading (typically 35 µA over the full range of output current, 0 mA to 150 mA). These two key specifications yield a significant improvement in operating life for battery-powered systems. This LDO also features a sleep mode; applying a TTL high signal to EN (enable) shuts down the regulator, reducing the quiescent current to less than 1 µA (typ).

Power good (PG) is an active-high output, which can be used to implement a power-on reset or a low-battery indicator.

TPS76533
DROPOUT VOLTAGE
vs
FREE-AIR TEMPERATURE



TPS76533
GROUND CURRENT
vs
LOAD CURRENT



The TPS765xx is offered in 1.5-V, 1.8-V, 2.5-V, 2.7-V, 2.8-V, 3-V, 3.3-V and 5-V fixed-voltage versions and in an adjustable version (programmable over the range of 1.25 V to 5.5 V). Output voltage tolerance is specified as a maximum of 3% over line, load, and temperature ranges. The TPS765xx family is available in an 8-pin SOIC package.

ORDERING INFORMATION(1)

T_A	V_O (TYP)	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	Adjustable	SOIC – D	Reel of 2500	TPS76501QDRQ1	76501Q

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

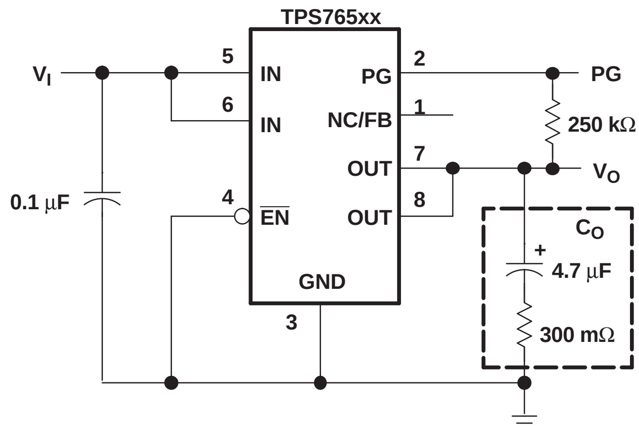
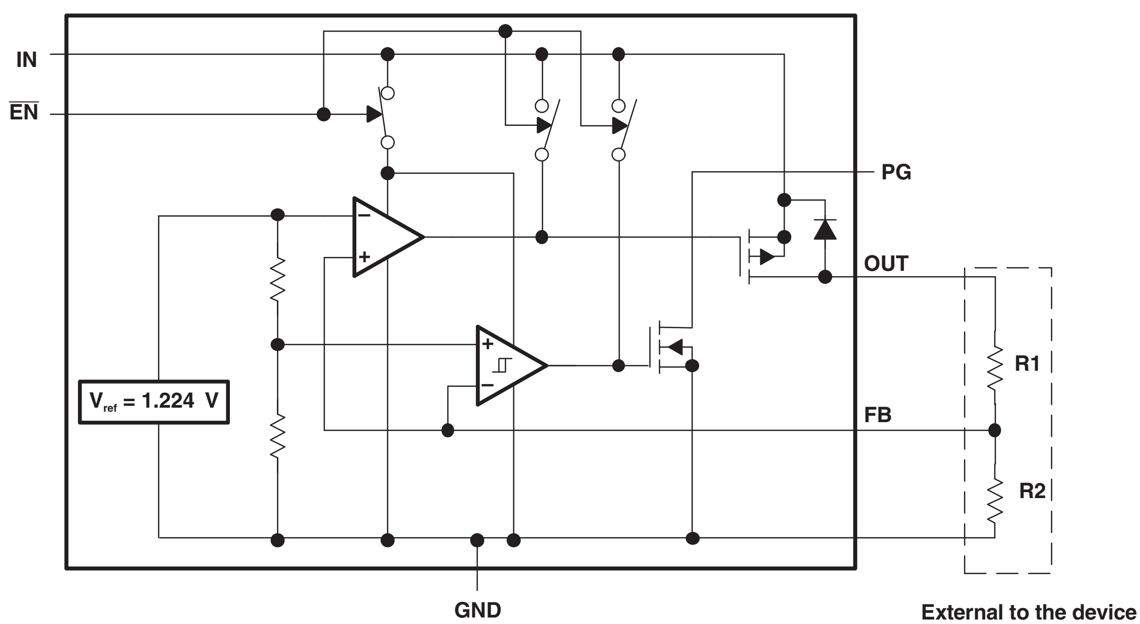
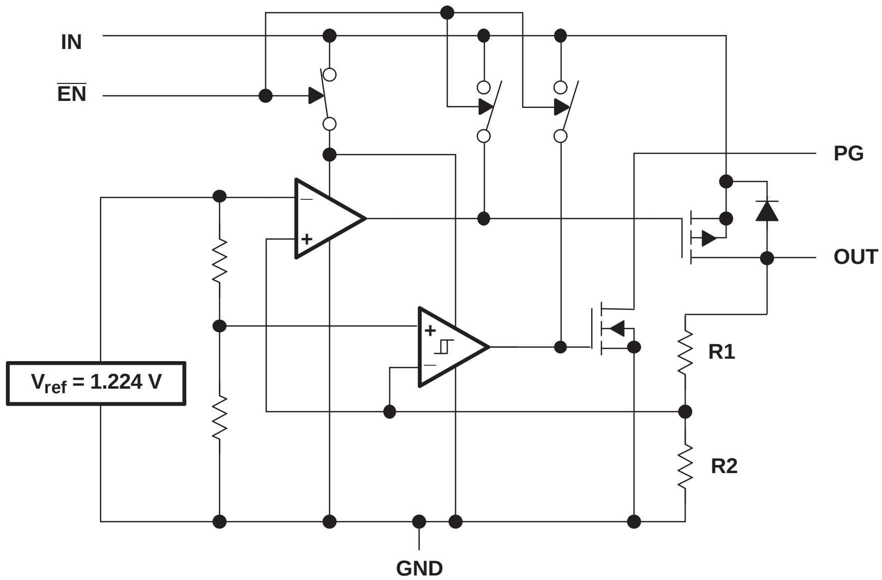


Figure 1. Typical Application Configuration for Fixed Output Options

FUNCTIONAL BLOCK DIAGRAM – ADJUSTABLE-VOLTAGE VERSION



FUNCTIONAL BLOCK DIAGRAM – FIXED-VOLTAGE VERSION



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
$\overline{EN}$	1	I	Enable
FB	2	I	Feedback voltage
GND	3		Regulator ground
IN	4, 5	I	Input voltage
OUT	6, 7	O	Regulated output voltage
PG	8	O	Power good output

ABSOLUTE MAXIMUM RATINGS[(1)(2)]

over operating free-air temperature range (unless otherwise noted)

			VALUE
V_I	Input voltage range		–0.3 V to 13.5 V
	Voltage range at $\overline{EN}$		–0.3 V to 16.5 V
	Maximum PG voltage		16.5 V
I_O	Peak output current		Internally limited
P_D	Continuous total power dissipation		See *Dissipation Ratings*
V_O	Output voltage (OUT, FB)		7 V
T_J	Operating virtual junction temperature range		–40°C to 125°C
T_{stg}	Storage temperature range		–65°C to 150°C
ESD	Electrostatic discharge rating	Human-Body Model	2000 V
		Machine Model	200 V
		Charged-Device Model	1500 V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network terminal ground.

DISSIPATION RATINGS

PACKAGE	AIR FLOW (CFM)	POWER RATING T_A < 25°C	DERATING FACTOR $T_A \geq$ 25°C	POWER RATING T_A = 70°C	POWER RATING T_A = 85°C
D	0	568 mW	5.68 mW/°C	312 mW	227 mW
	250	904 mW	9.04 mW/°C	497 mW	361 mW

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
V_I	Input voltage[(1)]	2.7	10	V
V_O	Output voltage	1.2	5.5	V
I_O	Output current[(2)]	0	150	mA
T_J	Operating virtual junction temperature	–40	125	°C

(1) To calculate the minimum input voltage for your maximum output current, use the following equation: $V_{I(min)} = V_{O(max)} + V_{DO(max\ load)}$.
(2) Continuous current and operating junction temperature are limited by internal protection circuitry, but it is not recommended that the device operate under conditions beyond those specified in this table for extended periods of time.

ELECTRICAL CHARACTERISTICS

$V_I = V_{O(typ)} + 1$ V, $I_O = 10$ µA, $\overline{EN} = 0$ V, $C_O = 4.7$ µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_J	MIN	TYP	MAX	UNIT
Output voltage[(1)]	TPS76501	10-µA to 150-mA load	5.5 V ≥ V_O ≥ 1.25 V	25°C		V_O		V
				–40°C to 125°C	0.97V_O		1.03V_O	
	TPS76515		2.7 V < V_{IN} < 10 V	25°C		1.5		
				–40°C to 125°C	1.455		1.545	
	TPS76518		2.8 V < V_{IN} < 10 V	25°C		1.8		
				–40°C to 125°C	1.746		1.854	
	TPS76525		3.5 V < V_{IN} < 10 V	25°C		2.5		
				–40°C to 125°C	2.425		2.575	
	TPS76527		3.7 V < V_{IN} < 10 V	25°C		2.7		
				–40°C to 125°C	2.619		2.781	
	TPS76528		3.8 V < V_{IN} < 10 V	25°C		2.8		
				–40°C to 125°C	2.716		2.884	
	TPS76530		4 V < V_{IN} < 10 V	25°C		3		
				–40°C to 125°C	2.910		3.090	
	TPS76533		4.3 V < V_{IN} < 10 V	25°C		3.3		
				–40°C to 125°C	3.201		3.399	
	TPS76550		6 V < V_{IN} < 10 V	25°C		5		
				–40°C to 125°C	4.850		5.150	
Quiescent current (GND current)[(1)]		10 µA < I_O < 150 mA		25°C		35		µA
		I_O = 150 mA		–40°C to 125°C			50	
Output voltage line regulation[(1)(2)] ($\Delta V_O/V_O$)		V_O + 1 V < V_I ≤ 10 V		25°C		0.01		%/V
Load regulation		I_O = 10 µA to 150 mA		–40°C to 125°C		0.3		%
Output noise voltage		BW = 300 Hz to 50 kHz, C_O = 4.7 µF		25°C		200		µVrms
Output current limit		V_O = 0 V		–40°C to 125°C		0.8	1.2	A
Thermal shutdown junction temperature						150		°C
Standby current		$\overline{EN} = V_I$, 2.7 V < V_I < 10 V		25°C		1		µA
				–40°C to 125°C			10	
FB input current	TPS76501	FB = 1.5 V		–40°C to 125°C		2		nA
High-level $\overline{EN}$ input voltage				–40°C to 125°C	2			V
Low-level $\overline{EN}$ input voltage				–40°C to 125°C			0.8	V
Power-supply ripple rejection[(1)]		f = 1 kHz, C_O = 4.7 µF, I_O = 10 mA		25°C		63		dB
PG	Minimum input voltage for valid PG	$I_{O(PG)}$ = 300 µA		–40°C to 125°C		1.1		V
	Trip threshold voltage	V_O decreasing		–40°C to 125°C	92		98	%V_O
	Hysteresis voltage	Measured at V_O		–40°C to 125°C		0.5		%V_O
	Output low voltage	V_I = 2.7 V, $I_{O(PG)}$ = 1 mA		–40°C to 125°C		0.15	0.4	V
	Leakage current	$V_{(PG)}$ = 5 V		–40°C to 125°C			1	µA
$\overline{EN}$ input current		$\overline{EN}$ = 0 V		–40°C to 125°C	–1	0	1	µA
		$\overline{EN} = V_I$			–1		1	

(1) Minimum IN operating voltage is 2.7 V or $V_{O(typ)}$ + 1 V, whichever is greater. Maximum IN voltage 10 V.
(2) If $V_O \le 1.8$ V then $V_{I(min)} = 2.7$ V, $V_{I(max)} = 10$ V:

$$\text{Line Regulation (mV)} = (\%/V) \times \frac{V_O(V_{I(max)} - 2.7\ V)}{100} \times 1000$$

If $V_O \ge 2.5$ V then $V_{I(min)} = V_O + 1$ V, $V_{I(max)} = 10$ V:

$$\text{Line Regulation (mV)} = (\%/V) \times \frac{V_O\left(V_{I(max)} - (V_O + 1\ V)\right)}{100} \times 1000$$

ELECTRICAL CHARACTERISTICS (continued)

$V_I = V_{O(typ)} + 1$ V, $I_O = 10$ µA, $\overline{EN} = 0$ V, $C_O = 4.7$ µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_J	MIN	TYP	MAX	UNIT
Dropout voltage(3)	TPS76528	$I_O = 150$ mA	25°C		190		mV
			–40°C to 125°C			330	
	TPS76530		25°C		160		
			–40°C to 125°C			280	
	TPS76533		25°C		140		
			–40°C to 125°C			240	
	TPS76550		25°C		85		
			–40°C to 125°C			150	

(3) IN voltage equals $V_{O(typ)}$ – 100 mV with output voltage set to 3.3 V nominal with external resistor divider. TPS76515, TPS76518, TPS76525, and TPS76527 dropout voltage limited by input voltage range limitations (i.e., TPS76530 input voltage must drop to 2.9 V for purpose of this test).

TYPICAL CHARACTERISTICS

Table of Graphs

		FIGURE
Output voltage	vs Load current	2, 3
	vs Free-air temperature	4, 5
Ground current	vs Load current	6, 7
	vs Free-air temperature	8, 9
Power-supply ripple rejection	vs Frequency	10
Output spectral noise density	vs Frequency	11
Output impedance	vs Frequency	12
Dropout voltage	vs Free-air temperature	13, 14
Line transient response		15, 17
Load transient response		16, 18
Output voltage	vs Time	19
Dropout voltage	vs Input voltage	20
Equivalent series resistance (ESR)(1)	vs Output current	21 through 24
Equivalent series resistance (ESR)(1)	vs Added ceramic capacitance	25, 26

(1) Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

TPS76533
OUTPUT VOLTAGE
vs
LOAD CURRENT

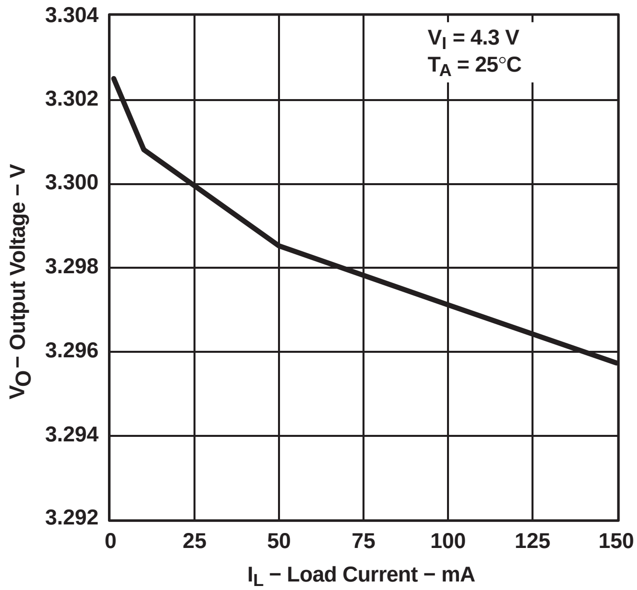


Figure 2.

TPS76515
OUTPUT VOLTAGE
vs
LOAD CURRENT

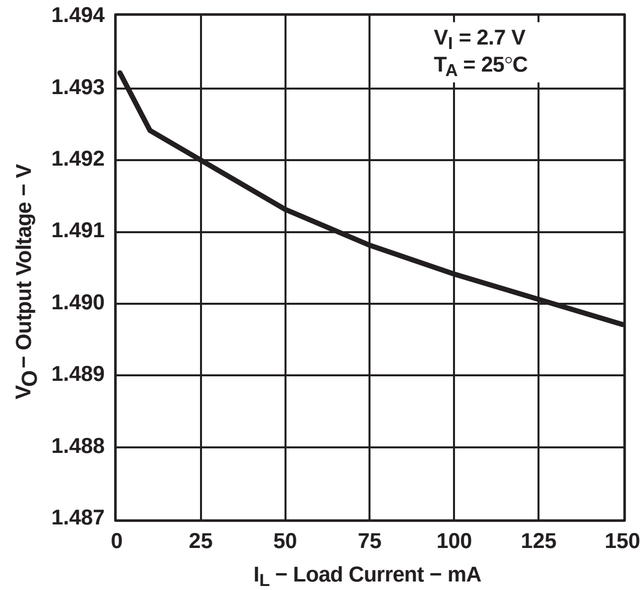


Figure 3.

TPS76533
OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

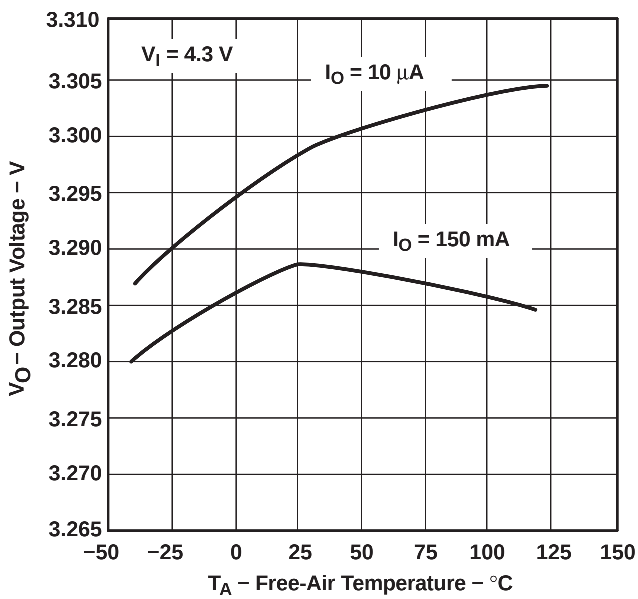


Figure 4.

TPS76515
OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

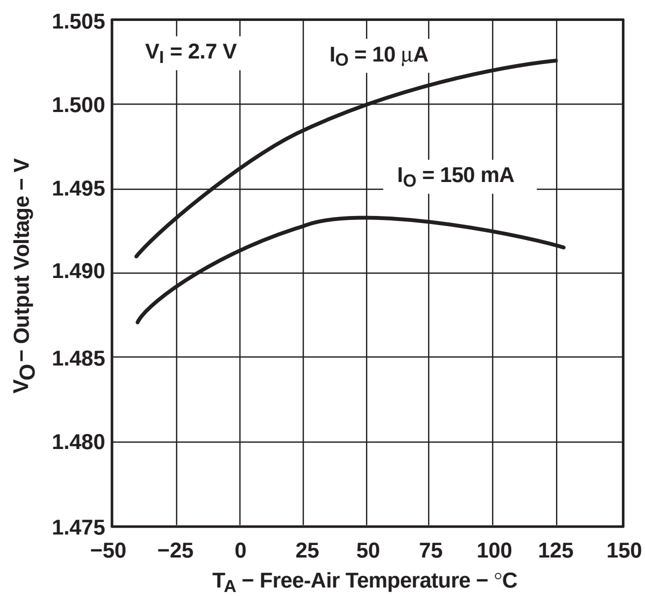


Figure 5.

TPS76533
GROUND CURRENT
vs
LOAD CURRENT

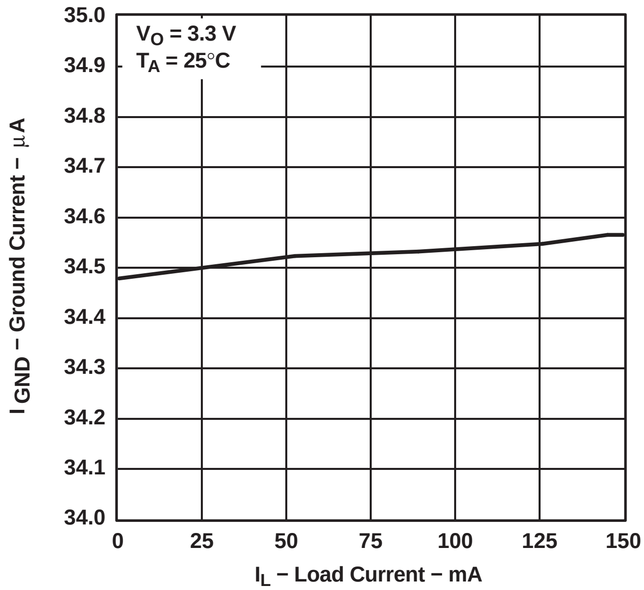


Figure 6.

TPS76515
GROUND CURRENT
vs
LOAD CURRENT

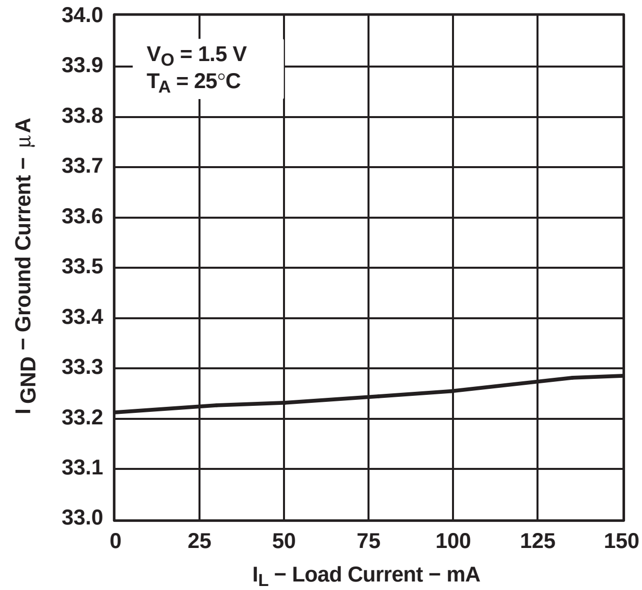


Figure 7.

TPS76533
GROUND CURRENT
vs
FREE-AIR TEMPERATURE

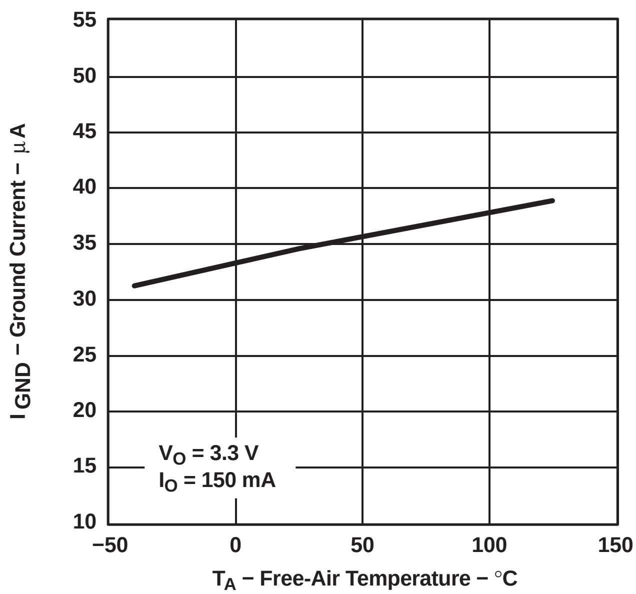


Figure 8.

TPS76515
GROUND CURRENT
vs
FREE-AIR TEMPERATURE

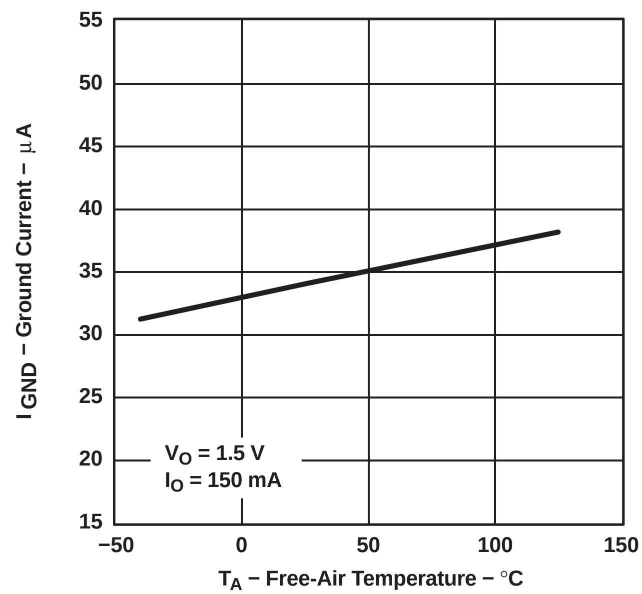


Figure 9.

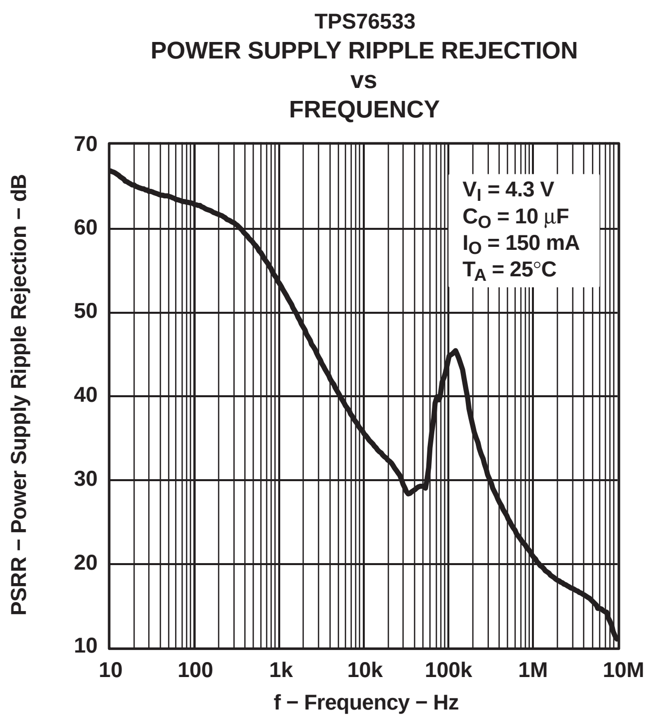


Figure 10.

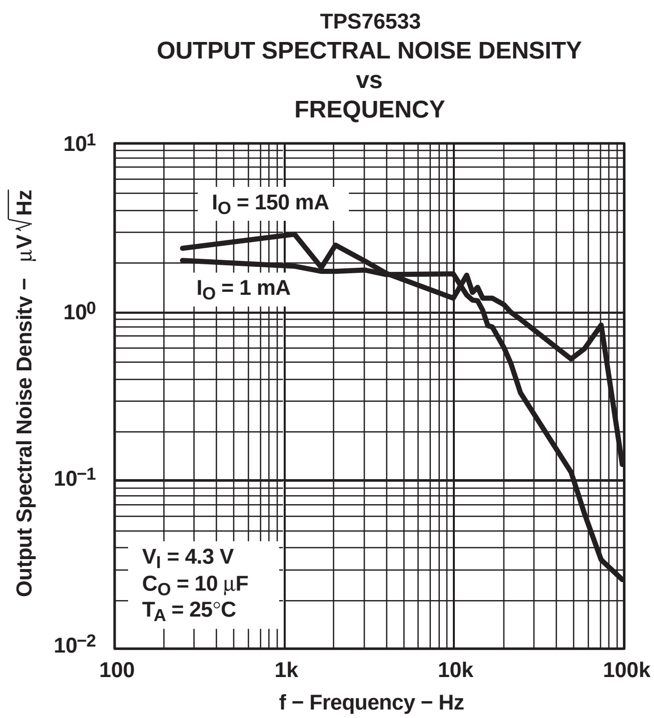


Figure 11.

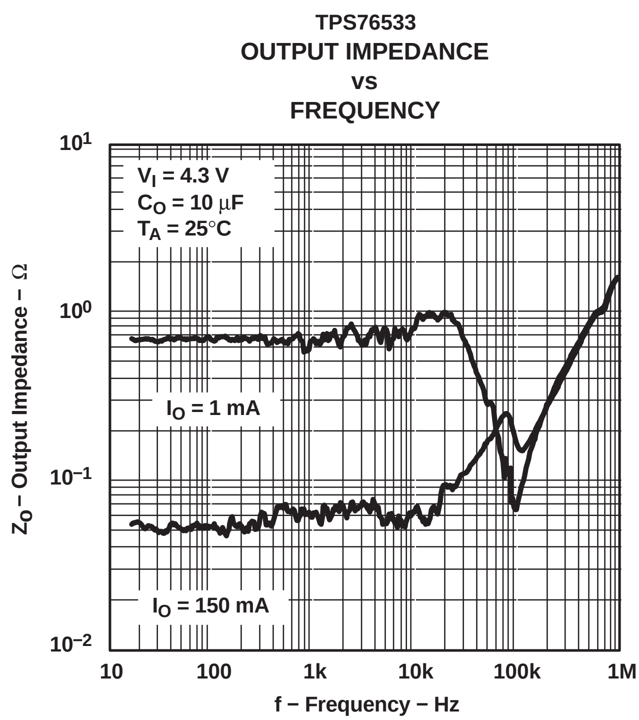


Figure 12.

TPS76550
DROPOUT VOLTAGE
vs
FREE-AIR TEMPERATURE

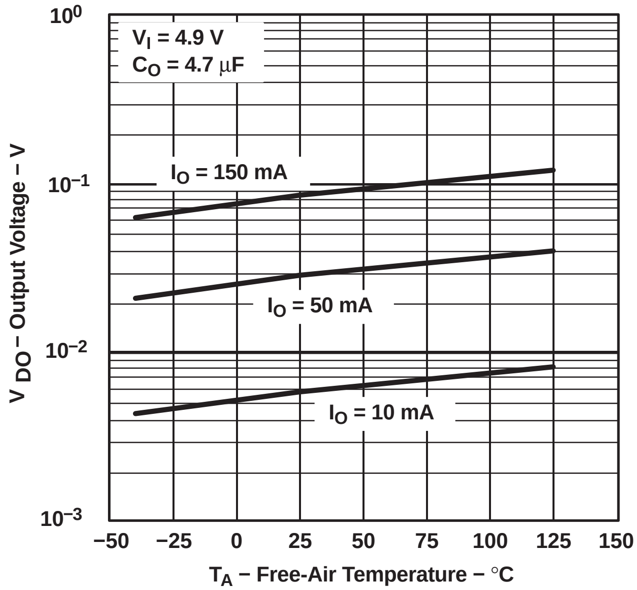


Figure 13.

TPS76533
DROPOUT VOLTAGE
vs
FREE-AIR TEMPERATURE

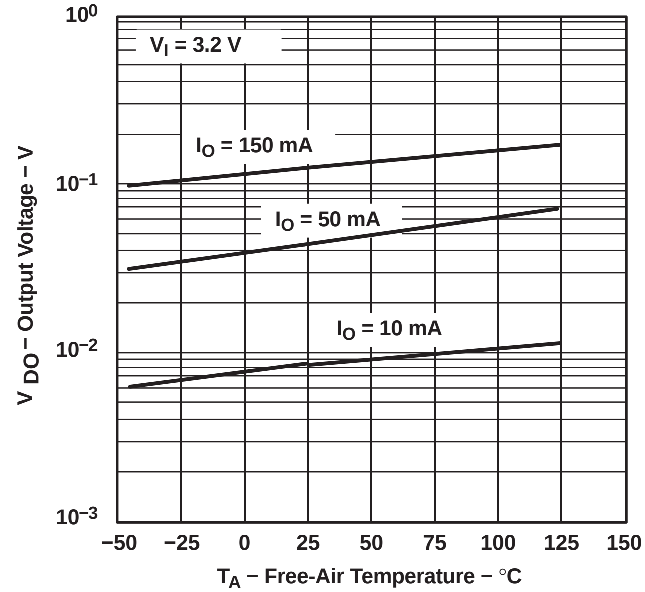


Figure 14.

TPS76515
LINE TRANSIENT RESPONSE

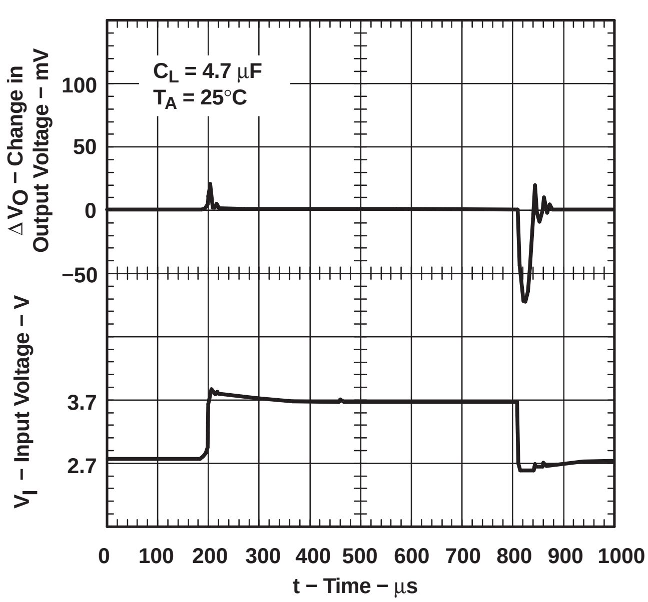


Figure 15.

TPS76515
LOAD TRANSIENT RESPONSE

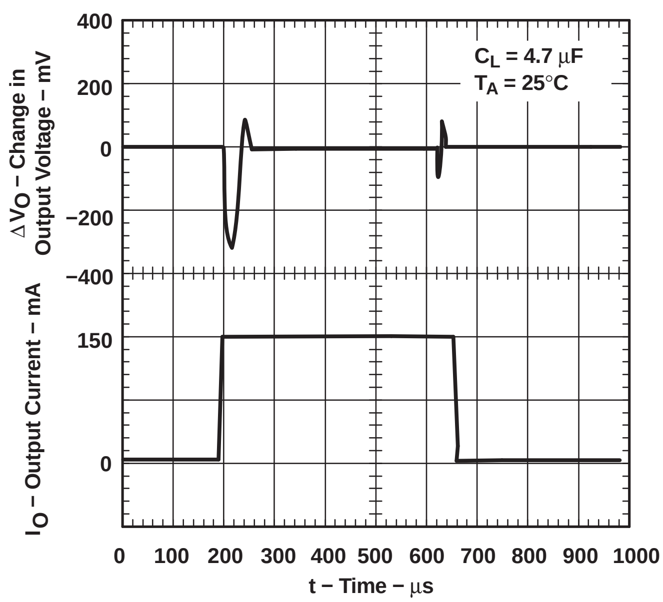


Figure 16.

TPS76533
LINE TRANSIENT RESPONSE

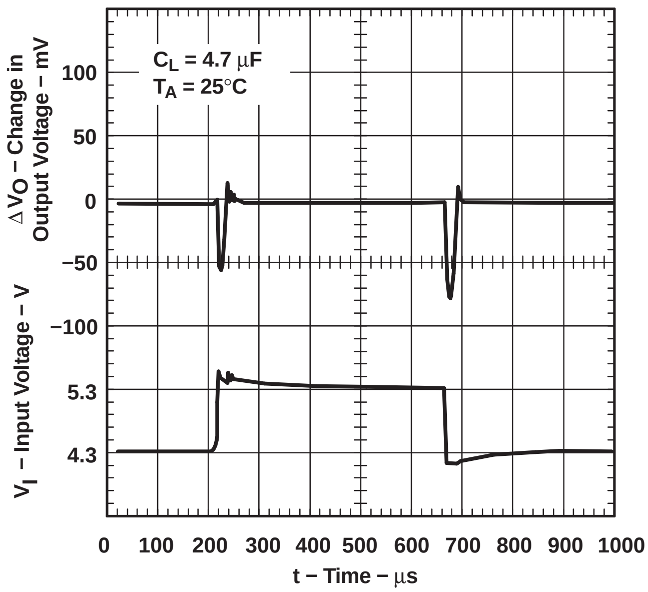


Figure 17.

TPS76533
LOAD TRANSIENT RESPONSE

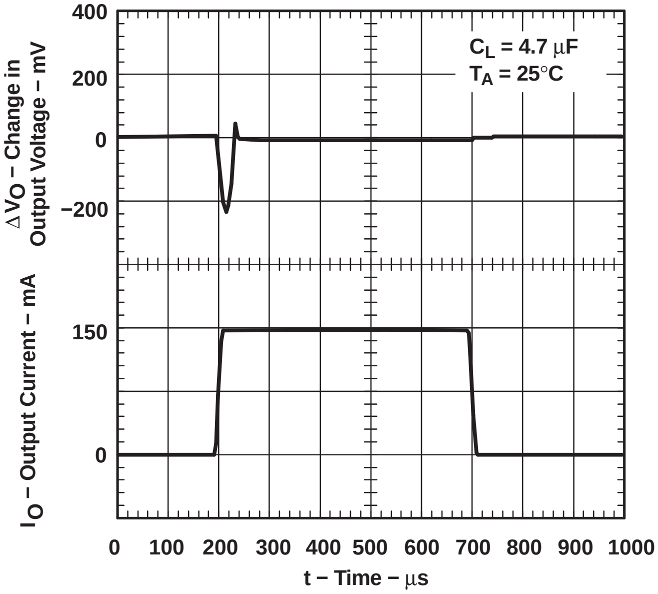


Figure 18.

TPS76533
OUTPUT VOLTAGE
vs
TIME (AT STARTUP)

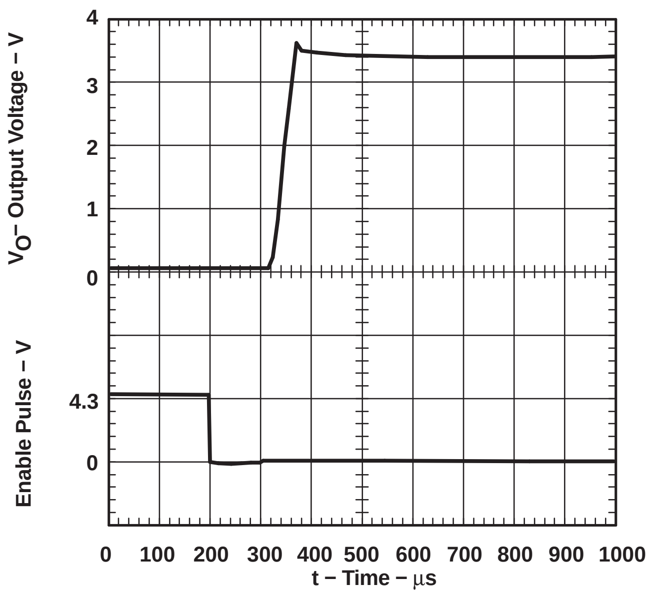


Figure 19.

TPS76501
DROPOUT VOLTAGE
vs
INPUT VOLTAGE

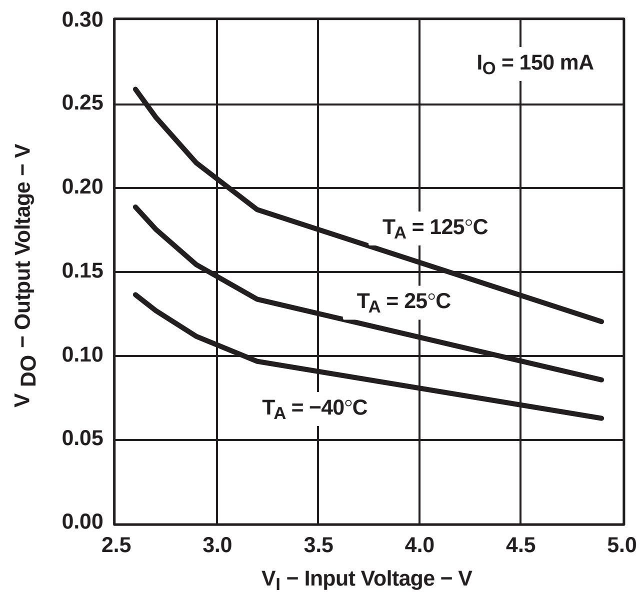


Figure 20.

TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE(1)
vs
OUTPUT CURRENT

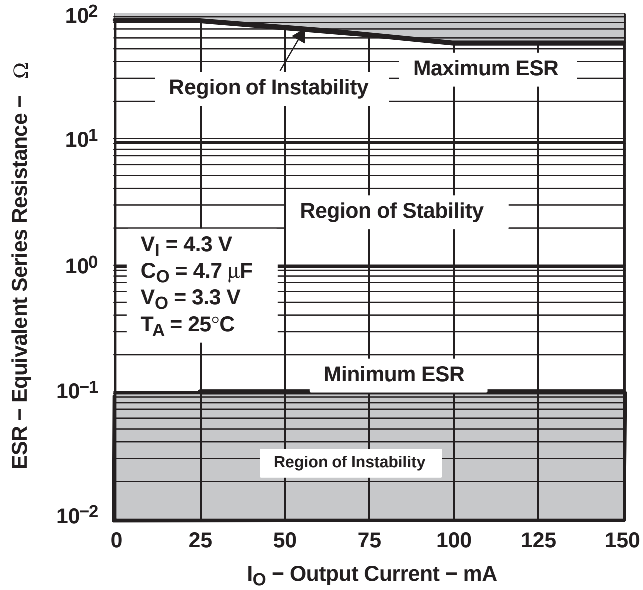


Figure 21.

TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE(1)
vs
OUTPUT CURRENT

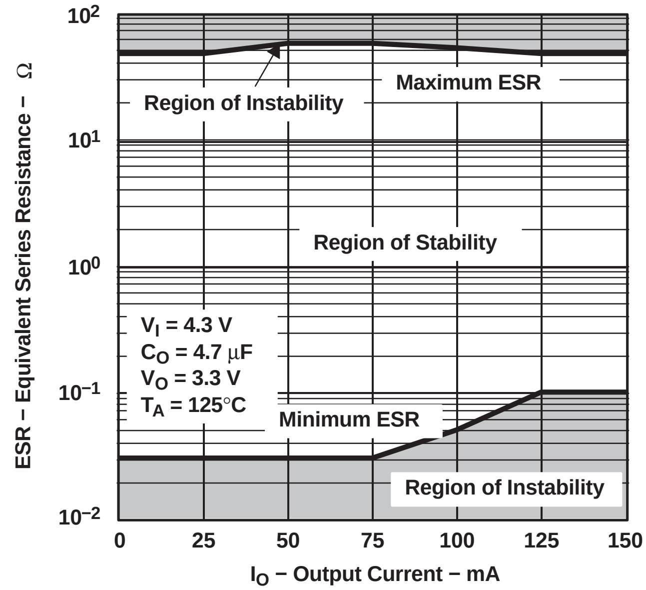


Figure 22.

TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE(1)
vs
OUTPUT CURRENT

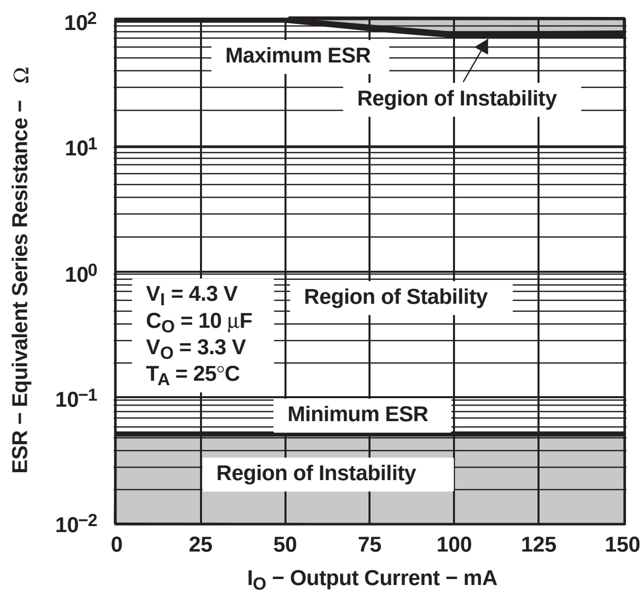


Figure 23.

TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE(1)
vs
OUTPUT CURRENT

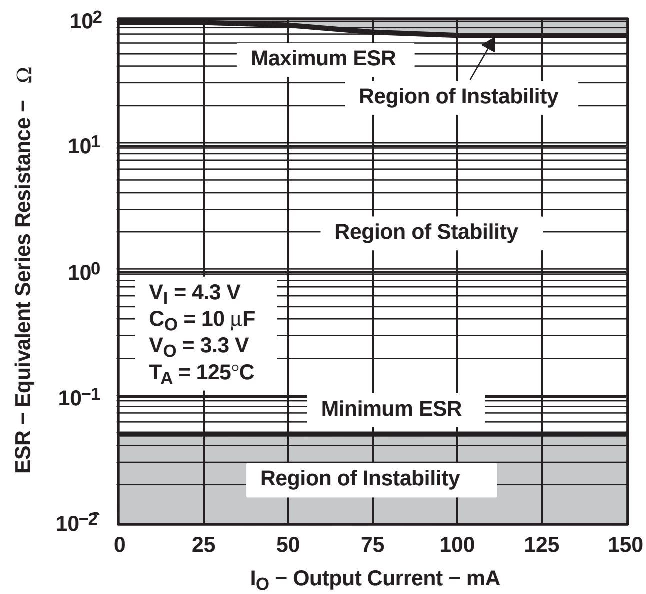


Figure 24.

(1) Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

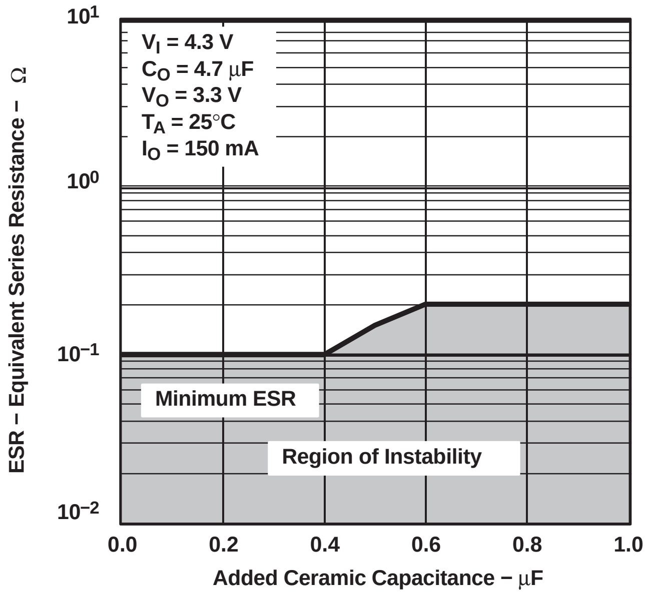


Figure 25.

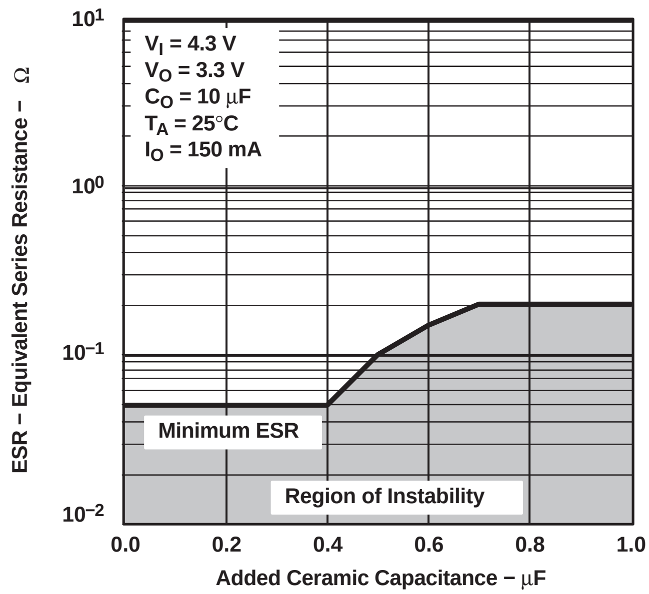


Figure 26.

(1) Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

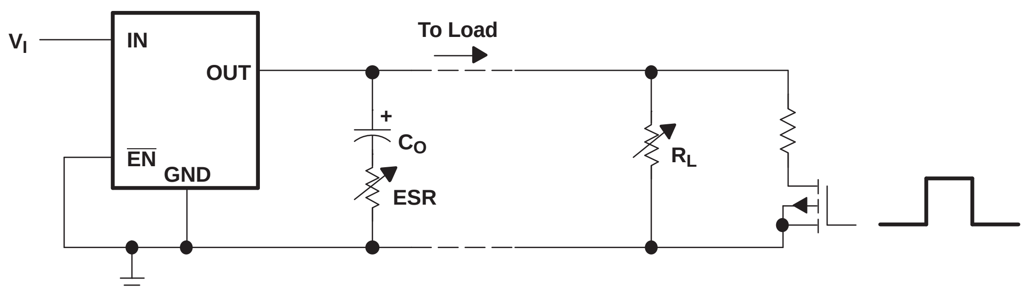


Figure 27. Test Circuit for Typical Regions of Stability (Figure 21 through Figure 24) (Fixed-Output Options)

APPLICATION INFORMATION

The TPS765xx family includes eight fixed-output voltage regulators (1.5 V, 1.8 V, 2.5 V, 2.7 V, 2.8 V, 3 V, 3.3 V, and 5 V), and an adjustable regulator, the TPS76501 (adjustable from 1.25 V to 5.5 V).

Device Operation

The TPS765xx features very low quiescent current, which remains virtually constant even with varying loads. Conventional LDO regulators use a pnp pass element, the base current of which is directly proportional to the load current through the regulator ($I_B = I_C/\beta$). The TPS765xx uses a PMOS transistor to pass current; because the gate of the PMOS is voltage driven, operating current is low and invariable over the full load range.

Another pitfall associated with the pnp-pass element is its tendency to saturate when the device goes into dropout. The resulting drop in β forces an increase in I_B to maintain the load. During power up, this translates to large start-up currents. Systems with limited supply current may fail to start up. In battery-powered systems, it means rapid battery discharge when the voltage decays below the minimum required for regulation. The TPS765xx quiescent current remains low even when the regulator drops out, eliminating both problems.

The TPS765xx also features a shutdown mode that places the output in the high-impedance state (essentially equal to the feedback-divider resistance) and reduces quiescent current to 1 µA (typ). If the shutdown feature is not used, $\overline{EN}$ should be tied to ground. Response to an enable transition is quick; regulated output voltage is reestablished in typically 160 µs.

Minimum Load Requirements

The TPS765xx is stable even at zero load; no minimum load is required for operation.

FB Pin Connection

The FB pin is an input pin to sense the output voltage and close the loop for the adjustable voltage. The output voltage is sensed through a resistor divider network to close the loop as it is shown in Figure 29. Normally, this connection should be as short as possible; however, the connection can be made near a critical circuit to improve performance at that point. Internally, FB connects to a high-impedance wide-bandwidth amplifier and noise pickup feeds through to the regulator output. Routing the FB connection to minimize/avoid noise pickup is essential.

External Capacitor Requirements

An input capacitor is not usually required; however, a ceramic bypass capacitor (0.047 µF or larger) improves load transient response and noise rejection if the TPS765xx is located more than a few inches from the power supply. A higher-capacitance electrolytic capacitor may be necessary if large (hundreds of milliamps) load transients with fast rise times are anticipated.

Like all LDO regulators, the TPS765xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance value is 4.7 µF and the ESR must be between 300 mΩ and 20 Ω. Capacitor values 4.7 µF or larger are acceptable, provided the ESR is less than 20 Ω. Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described previously.

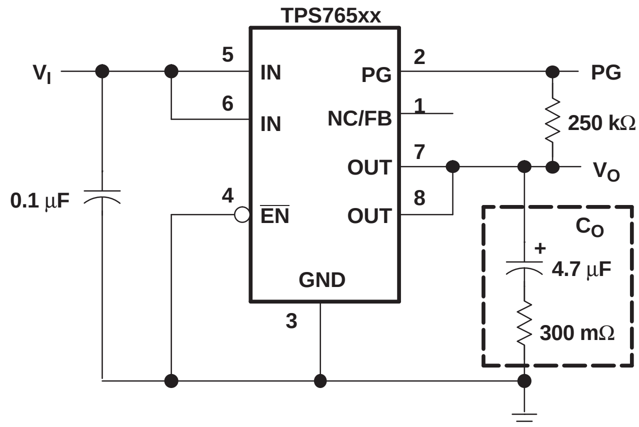


Figure 28. Typical Application Circuit (Fixed Versions)

Programming the TPS76501 Adjustable LDO Regulator

The output voltage of the TPS76501 adjustable regulator is programmed using an external resistor divider as shown in Figure 29. The output voltage is calculated using Equation 1:

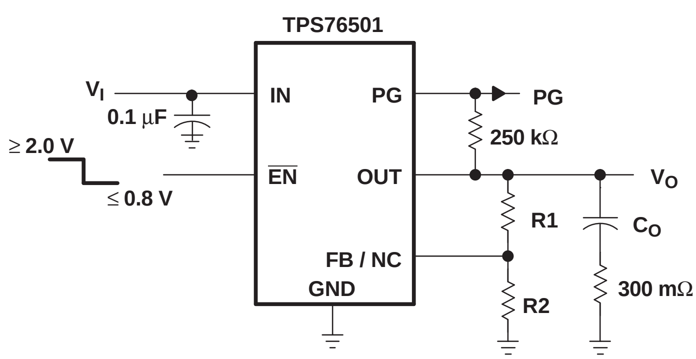
$$V_O = V_{ref} \times \left(1 + \frac{R1}{R2}\right) \tag{1}$$

Where

V_{ref} = 1.224 V (typ) (the internal reference voltage)

Resistors R1 and R2 should be chosen for approximately 7-μA divider current. Lower-value resistors can be used but offer no inherent advantage and waste more power. Higher values should be avoided as leakage currents at FB increase the output voltage error. The recommended design procedure is to choose R2 = 169 kΩ to set the divider current at 7 μA and then calculate R1 using Equation 2:

$$R1 = \left(\frac{V_O}{V_{ref}} - 1\right) \times R2 \tag{2}$$



OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE	R1	R2	UNIT
2.5 V	174	169	kΩ
3.3 V	287	169	kΩ
3.6 V	324	169	kΩ
4.0 V	383	169	kΩ
5.0 V	523	169	kΩ

Figure 29. TPS76501 Adjustable LDO Regulator Programming

Power-Good Indicator (PG)

The TPS765xx features a power-good output that can be used to monitor the status of the regulator. The internal comparator monitors the output voltage: when the output drops to between 92% and 98% of its nominal regulated value, the PG output transistor turns on, taking the signal low. The open-drain output requires a pullup resistor. If not used, it can be left floating. PG can be used to drive power-on reset circuitry or used as a low-battery indicator.

Regulator Protection

The TPS765xx PMOS-pass transistor has a built-in back diode that conducts reverse currents when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. When extended reverse voltage is anticipated, external limiting may be appropriate.

The TPS765xx also features internal current limiting and thermal protection. During normal operation, the TPS765xx limits output current to approximately 0.8 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 150°C (typical), thermal-protection circuitry shuts it down. Once the device has cooled below 130°C (typical), regulator operation resumes.

Power Dissipation and Junction Temperature

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA}}$$

Where

T_{Jmax} is the maximum allowable junction temperature.
$R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package.
T_A is the ambient temperature.

The regulator dissipation is calculated using:

$$P_D = \left(V_I - V_O\right) \times I_O$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation triggers the thermal protection circuit.

PACKAGING INFORMATION

Orderable Device	Status [(1)]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [(2)]	Lead/Ball Finish	MSL Peak Temp [(3)]
TPS76501QDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[(1)] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[(2)] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[(3)] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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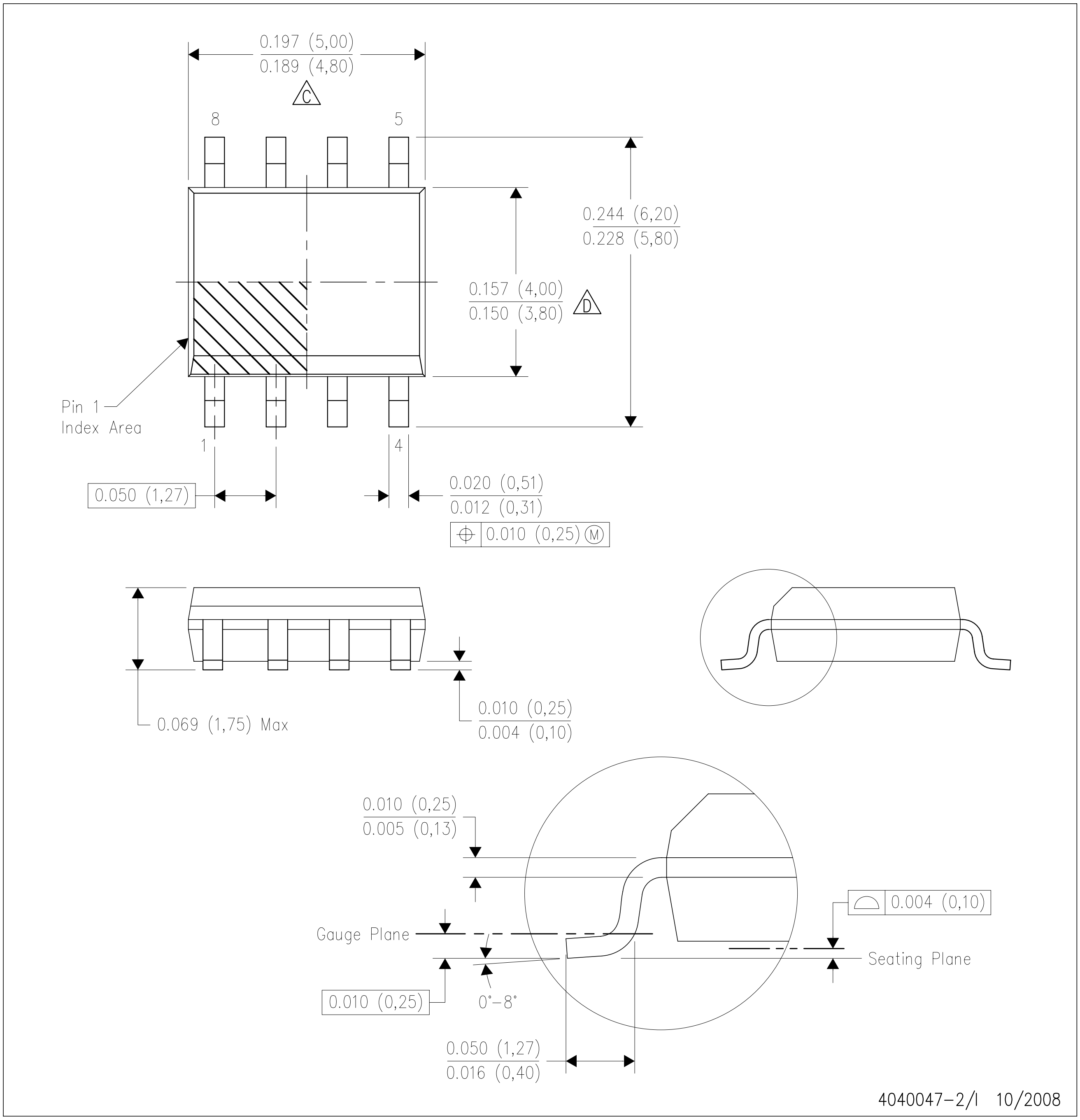
OTHER QUALIFIED VERSIONS OF TPS76501-Q1 :
- Catalog: TPS76501

NOTE: Qualified Version Definitions:
- Catalog - TI's standard catalog product

D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS-012 variation AA.

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